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THIN CHANNEL FET WITH RECESSED SOURCE/DRAINS AND EXTENSIONS

Abstract

A field effect transistor (FET), integrated circuit (IC) chip including the FETs and a method of forming the FETS. The devices have a thin channel, e.g., an ultra-thin (smaller than or equal to 10 nanometers (10nm)) silicon on insulator (SOI) layer. Source/drain regions are located in recesses at either end of the thin channel and are substantially thicker (e.g., 30nm) than the thin channel. Source/drain extensions and corresponding source/drain regions are self aligned to the FET gate and thin channel.